A' contd

2. (Once Amended) The MOSFET logic circuit as in claim 1, wherein the three transistors include first and second PMOS transistors and one NMOS transistor.

4. (Once Amended) The MOSFET logic circuit as in claim 1, wherein the first input signal is provided to a source of first and second transistors of the three transistors, the second input signal is provided to a gate of the second transistor, and a complement of the second input signal is provided to a gate of the first transistor.

5. (Once Amended) The MOSFET logic circuit as in claim 1, wherein a complement of the second input is provided to a gate of a third transistor of the three transistors.

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6. (Once Amended) The MOSFET logic circuit as in claim 1, wherein the at least two input signals to the first and second transistors further comprise a complement of the second input signal.

7. (Once Amended) The MOSFET logic circuit as in claim 1, wherein when the second input signal has a logic LOW level the output of the MOSFET logic circuit is an output signal of the transmission gate.

8. (Once Amended) The MOSFET logic circuit as in claim 1, wherein a third transistor of the three transistors is a pull-up transistor, and when the second input signal has a logic HIGH level the output of the MOSFET logic circuit has a voltage level approximately equal to a drain of the third transistor, which pulls up the output signal from the transmission gate to a logic